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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/506,033	02/16/2000	Yasushi Kubota	49087-CIP(820)	5865

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EDWARDS & ANGELL, LLP  
P.O. BOX 9169  
BOSTON, MA 02209

EXAMINER

TRAN, HENRY N

ART UNIT

PAPER NUMBER

2674

DATE MAILED: 07/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/506,033

Applicant(s)

KUBOTA ET AL.

Examiner

HENRY N. TRAN

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 April 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-3, 18-21, 37-53 and 58-64 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.

- 6) ☒ Claim(s) 1-3, 18-21, 37, 53 and 58-64 is/are rejected.

- 7) ☒ Claim(s) 38-52 is/are objected to.

- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 February 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☒ Certified copies of the priority documents have been received in Application No. 09/300,178.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

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### DETAILED ACTION

This Office action is in response to the applicant's amendment received 4/25/0 (paper no. 9). The amendments to the specification and the claims have been entered; and the applicant's remarks were considered, with the results set forth as following.

1. Claims 1-3, 18-21, 37-53, and 58-64 are pending in this application.

#### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 18-21, 37, 53, 58-64 are rejected under 35 U.S.C. 102(e) as being anticipated by Isami et al (U.S. Patent 6,166,725)

4. Regarding claim 1, Isami et al. teach a latch circuit 530 (a drain driver 530) for synchronizing a display data signal with a clock signal, comprising: a first input 533 (a bus line 533) comprising display data as the pulse signal (see figure 13; column 3, lines 3-4); a second input 532 comprising display data latch clock (D2) for latching display data; and an output circuit 557 for outputting LC driving voltages as the pulse signal in synchronization with the clock signal (see column 2, lines 62-65; col. 3, lines 3-4; col. 10, lines 4-7); wherein the fixed common-electrode voltage method has disadvantages that an amplitude of a voltage applied to

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the pixel electrode is twice that of the common-electrode voltage inversion method (column 5, lines 11-15) corresponding to the clock signal or the pulse signal having amplitude smaller than the amplitude of the pulse signal outputted from the latch circuit.

5. Regarding claims 2 and 3, Isami et al. further teach that the latch circuit 530 is supplied with a power potential 520 (column 3, lines 43-48), and an element (D1) (an output timing control clock D1) for holding display voltages in the storage register 555 (column 6, lines 5-10); and further comprising: a first circuit 555 (a storage register 555) for holding display voltages, and a second circuit 556 (a level shifter 556) for level shifting function, the first and second circuits being constructed so as to own some common elements of a semiconductor integrated circuit (LSI) (see figure 19, column 2, lines 62-63).

6. Regarding to claims 18, Isami et al teach a shift register 153 (figure 1), a plurality of latch circuits (165) , a clock signal and a frame start indicating signal (figure 13) corresponding to the latch circuits each internally having a clock signal control section for executing control to input and stop the supplied clock signal, and the fixed common-electrode voltage method has disadvantages that an amplitude of a voltage applied to the pixel electrode is twice that of the common-electrode voltage inversion method (column 5, lines 11-15) corresponding to the clock signal or the pulse signal having amplitude smaller than the amplitude of the pulse signal outputted from the latch circuit.

7. Regarding claims 19-21, Isami further also teach that: (i) the latch circuit 530 (the drain driver 530) based on control signals such as a clock signal, a display timing signal, a horizontal sync signal, and a vertical sync signal and a display signal transmitted from the main computer (column 2, lines 62-67), wherein a common electrode voltages is a predetermined clock signal

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(figures 17 and 18); (ii) a carry output from the drain driver 530 in one stage is inputted as a carry input to the drain driver 530 on the next stage, and latching operation of the data latch circuit of the drain driver 530 is controlled by the carry signal to prevent wrong display data from being written into the data latch circuit (column 3, lines 13-18).

8. Regarding claims 37, which is similar to the base claim 1, rephrased to emphasized that the latch circuit is a CMOS logical circuit, and the pulse signal is a first input signal having a first amplitude and the second input is a second input signal having a second amplitude, and is therefore rejected on the same reasons set forth in claim 1.

9. Regarding claims 53 and 58-64, Isami et al still further teach a TFT-LCD comprising a matrix of a plurality of pixels, each is a polysilicon TFT, surrounded with drain lines and gate lines, data signal line drive circuit 230 for supplying a video data signal to the data signal line, and a scanning signal line drive circuit 240 for supplying a scanning signal to the scanning signal lines (see figure 4); wherein the circuits 230 and 240 are formed on driving circuit boards (PCB1, PCB2) disposed along the peripheral of the TFT-LCD (see figure 15; column 3, line 61 to column 4, line 8); the TFT is an active element formed through a process at a temperature of not higher than 600 degree Celsius which is well known; the use of a pulse width modulation control for controlling the pulse width of the output pulse of the shift register circuit for driving the scanning and signal circuits for providing gray scale or color TFT-LCD is old and well-known in the art. Claims 53 and 58-64 are dependent upon the base claim 37, and are therefore rejected on the same reasons set forth for claim 37, and by the reasons noted above.

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***Allowable Subject Matter***

10. Claims 38-52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Arguments***

11. Applicant's arguments, see pages 13-14 of the amendment, filed 4/25/03, with respect to the rejection(s) of claim(s) 1-19 and 38-41 under 35 USC 112, second paragraph, have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Isami et al as discussed above.

***Conclusion***

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See form PTO-892.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HENRY N. TRAN whose telephone number is (703) 308-8410. The examiner can normally be reached on Mon - Fri from 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RICHARD A. HJERPE, can be reached at (703) 305-4709.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

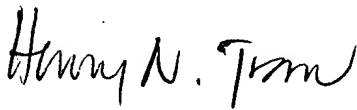
**or faxed to:**

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**(703) 872-9314 (for technology Center 2600 only)**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,  
Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding  
should be directed to the Technology Center 2600 Customer Service Office Whose telephone  
number is (703) 306-0377.



HENRY N. TRAN  
Examiner  
Art Unit 2674

hnt  
July 8, 2003